Silicon Carbide Thyristor Development to Optimize High-Power System SWaP

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Defense Systems Information Analysis Center

DEVCOM ARMY RESEARCH LABORATORY

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OUTLINE

- Research Motivation
- Silicon Carbide (SiC) for High Voltage, High Current
- Technical Challenges
- ARL Approach and Capabilities
- Device Overview
- Evaluation Methods
- Fast-Pulse Switching Results
- Key Takeaways

RESEARCH MOTIVATION

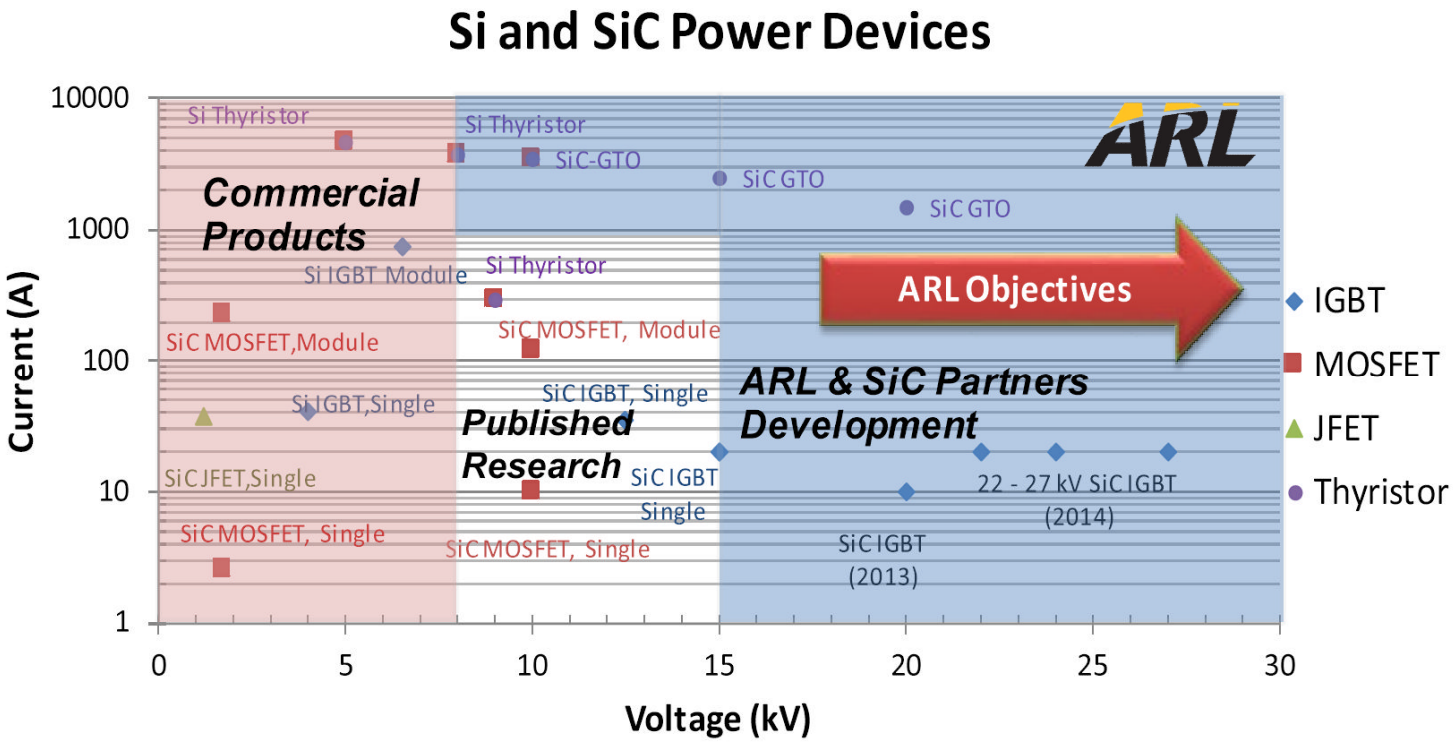
- U.S. Army Combat Capabilities Development Command (CCDC) Army Research Laboratory (ARL) conducts disruptive foundational research in support of Army modernization.

- Advancing components for high-power transmission and pulsed power enhances mission capability (mobility, survivability, & lethality) of Army high-priority modernization programs (Air & Missile Defense, Future Vertical Lift, & Next-Generation Combat Vehicle) by expanding high-power range, increasing power density, and maximizing efficiency of switching components.

- By driving high-voltage SiC device design and fully understanding and validating devices' capabilities relevant to Army needs, ARL can innovate new solutions for the future Army.

Versatile tactical power for survivability & lethality, multidomain dominance

RESEARCH MOTIVATION

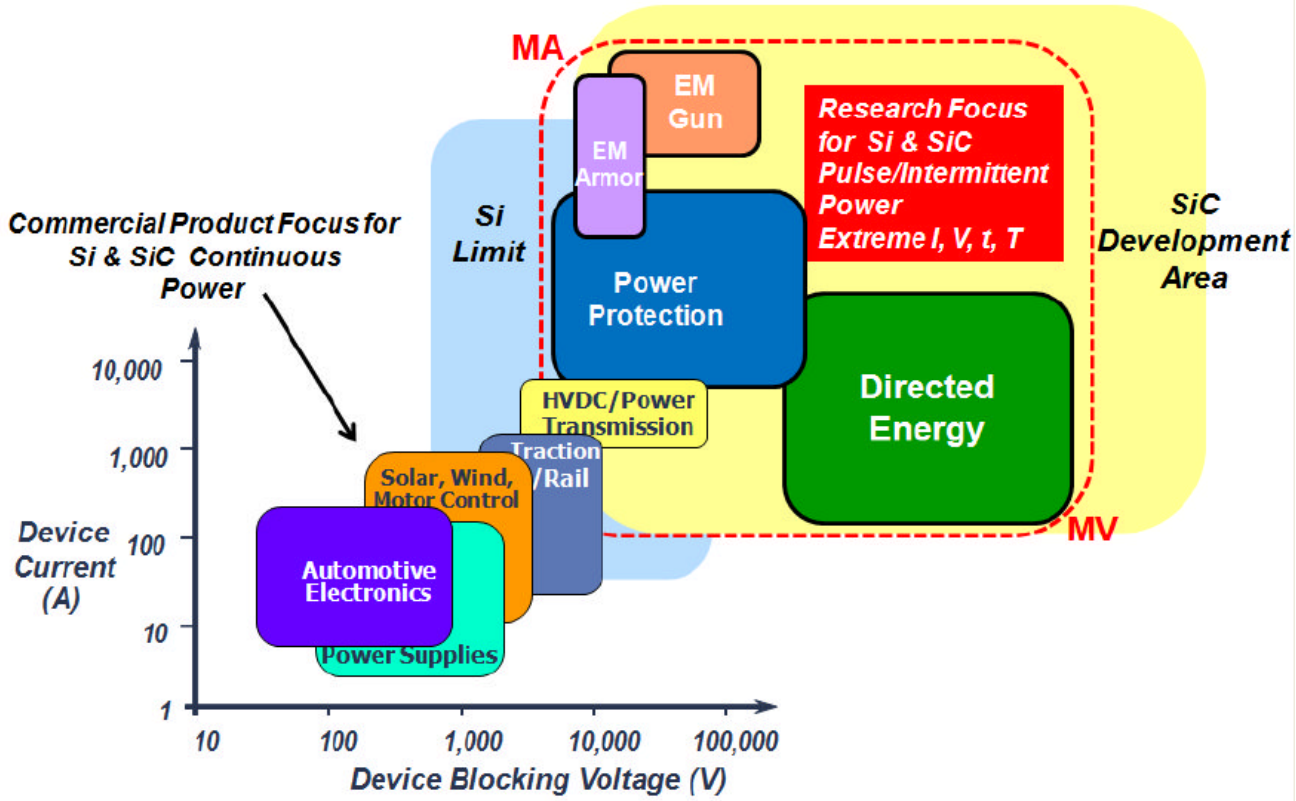


- SiC continues to be the most promising, near-term, wide band gap (WBG) semiconductor replacements for traditional Si-based power solutions.
- SiC is also the most promising, near-term WBG material to push forward into the high-voltage regime (>10 kV) — enabling new capabilities.
- ARL and research partners are focused on optimizing design at the chip level and propelling packaging innovation for high-voltage, power-dense modules.

SiC FOR HIGH VOLTAGE, HIGH CURRENT

Benefits of SiC Over Si

- Higher breakdown electric field (thinner epilayer, narrower termination)
- Lower R_{ON} and switching losses at very high-current density (greater efficiency)
- Good thermal conductivity (simpler cooling system, more thermal margin)
- High Young's modulus (withstand thermal transients of pulse stresses)
- Higher saturated drift velocity (supports high *dI/dt* and *dV/dt* capabilities)

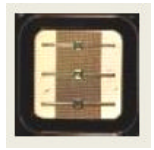


High voltage combined with pulsed high current is our unique research focus.

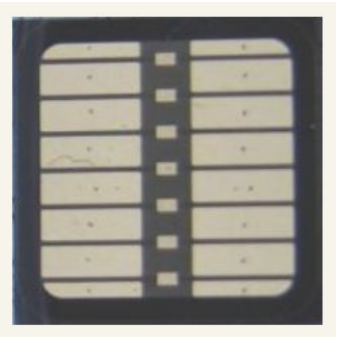
TECHNICAL CHALLENGES

Device Design Challenges

- Material thickness/purity/uniformity
- Trade-offs to increasing high voltage & chip size
- Fabrication complexity

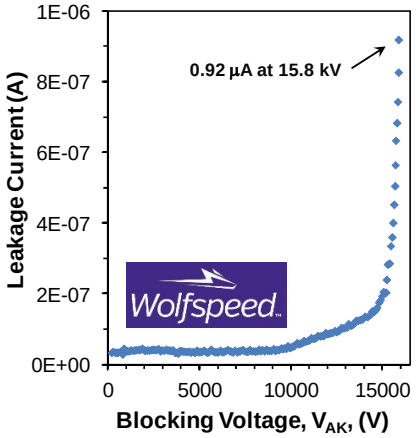


3 kV, 0.16 cm²

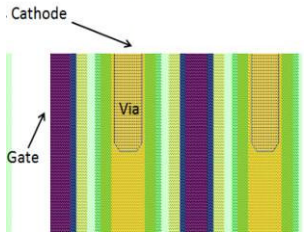


15 kV, 1 cm²

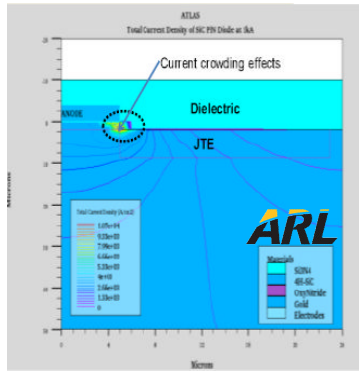
Device Characterization Challenges



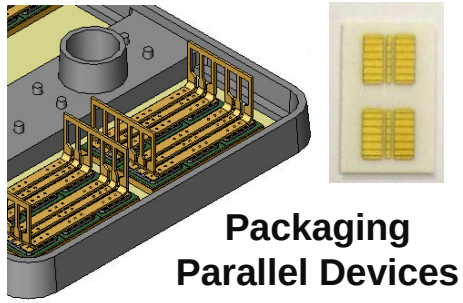
Higher Voltage



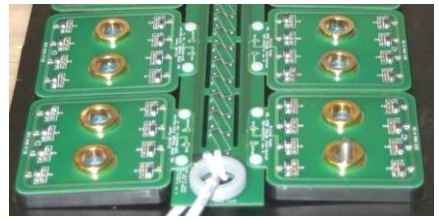
Higher Current Density



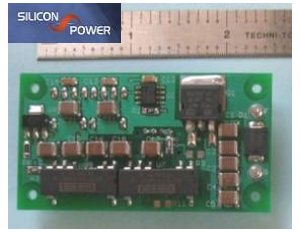
Modeling Transient Behavior

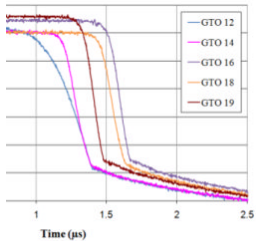


Packaging Parallel Devices



Parallel Bussing





Turn-on Control

APPROACH

- *Partner* with industry and universities to drive innovation in single-die device design, fabrication, packaging, controls for pulsed power, and low-duty cycle continuous power Army applications.

- Fully *characterize and analyze* device behavior at extreme electrical stresses *to gain deeper understanding* of semiconductor physics and design scalability.

- Directly compare different, novel device designs to determine advantages of each and how to further *optimize* epi thickness, material doping, chip layout, and processing.

CURRENT ARL HIGH-VOLTAGE DEVICE PROGRAM PARTNERS

Cree-Wolfspeed

- Previous programs (2012-2016) invested in epi fabrication & investigated designs for high-voltage **insulated-gate bipolar transistors (IGBTs), metal-oxide-semiconductor field-effect transistors (MOSFETs), thyristors, & diodes.**
- New program focus is to further develop **IGBTs** (>20 kV, 30 A) and **thyristors** (>15 kV, 50 A continuous or 5 kA pulsed).

SUNY-Poly

- Focus on 12-kV, 20-A **MOSFETs** with Prof. Woongje Sung.
- Leveraging state-of-the art capabilities of New York's Power Electronics Manufacturing Consortium.

GeneSiC

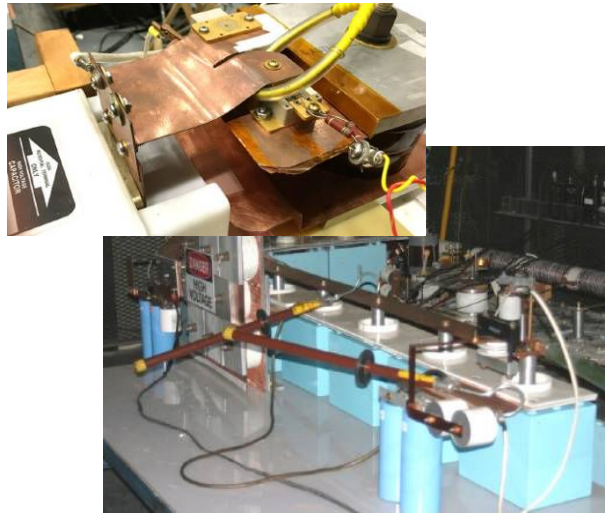
- Focus on 15-kV, 20-A **MOSFETs** & 20-kV, 40-A **IGBTs.**
- Leveraging previous work under the U.S. Department of Energy (DoE).
- Will utilize X-Fab (leveraging DoE's Power America).
- Consortium with Ohio State and the Nuclear Reactor Laboratory.

ARL DEVICE CHARACTERIZATION CAPABILITIES

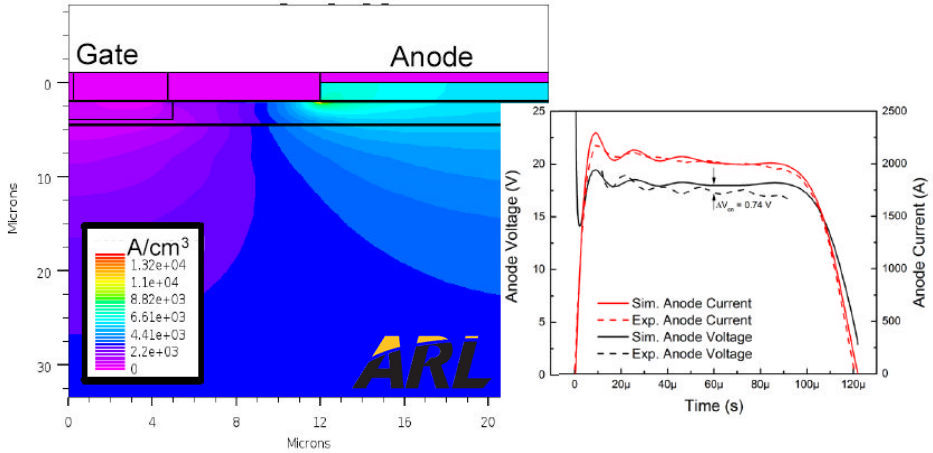
ARL has custom, high-voltage, high-current test capabilities highly relevant to Army-fielded conditions. Evaluation capabilities include:

- DC blocking voltage to 30 kV
- Pulsing >100 kA, widths ranging from 500 ns to 1 ms
- 10-kHz, step-down buck converter (10 kV to 2 kV)

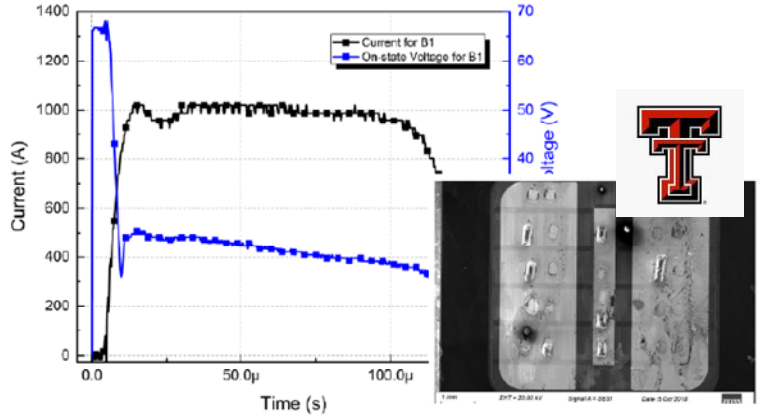
Ability to test at very high-pulsed current density has led to many insights, which steered significant improvements in device design and major changes to component packaging methods and materials used.



Evaluation circuits



Device simulation: static characteristics, dynamic switching, circuit behavior

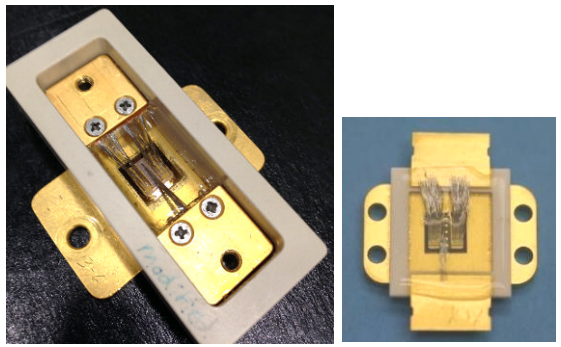


Texas Tech partnership: long-term, low-duty switching & analysis, thermal imaging, scanning electron microscope, focused ion beam, package simulation & analysis

EXPERIMENTAL FOCUS

For high-power EM systems, need to understand device operation over:

- High-voltage transients
- High-current densities
- Large-chip areas
- Turn-on process
- Turn-off process



15 kV, 1 cm² and 6 kV, 0.5 cm² super gate turn-off thyristors (SGTOs)

Understanding behavior at faster switching conditions is relevant to:

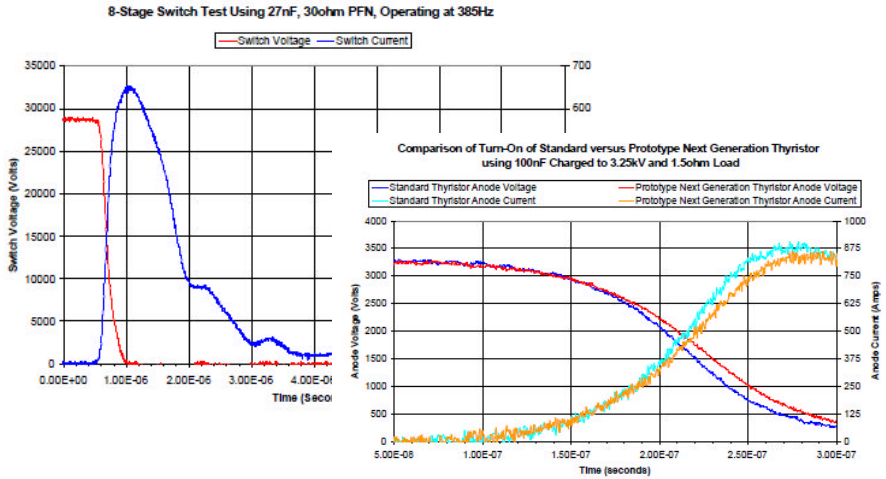
(1) Explore broader application space for high-voltage SiC diodes and thyristors.

(2) Investigate consequences or trade-offs to increasing high voltage and chip size.

(3) Optimizing device design for a wide range of switching conditions.

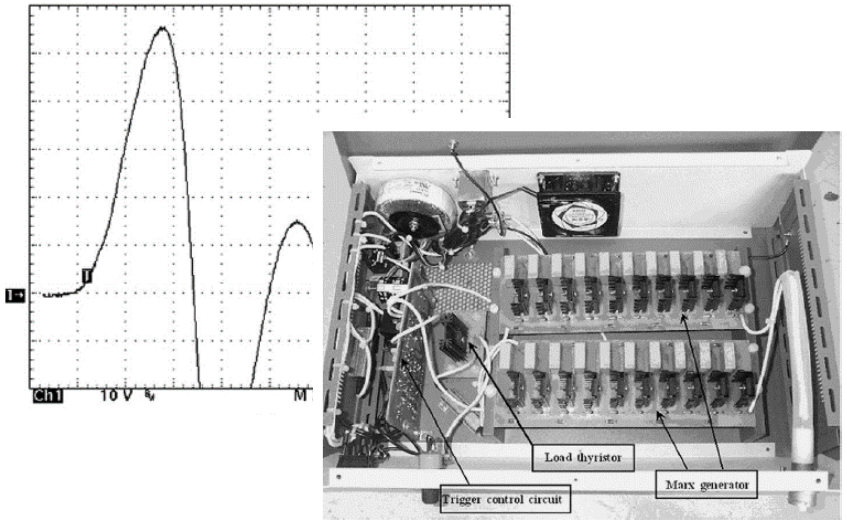
POSSIBLE APPLICATION SPACE

Replacing Thyratron for Pulsed Driver



Sanders. “Solid state switches for high-frequency operation as thyratron replacements,” www.appliedpulsepower.com, 2013.

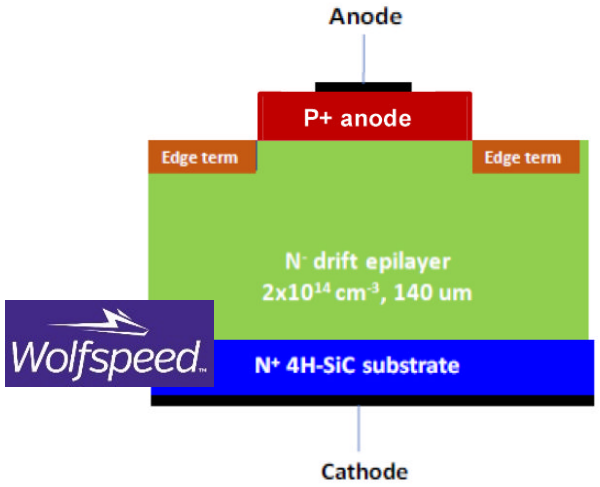
Reducing Stages of Marx High-Voltage Generator



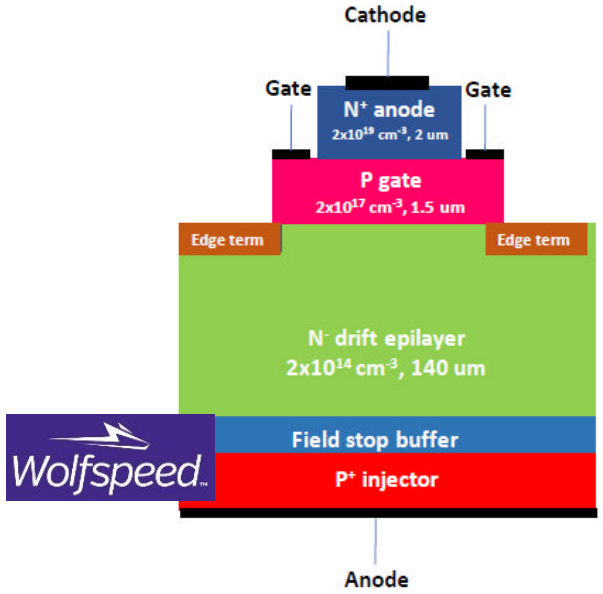
Pécastaing. “Very Fast Rise-Time Short-Pulse High-Voltage Generator,” IEEE Trans. Plasma Science, 2006.

THYRISTOR AND PIN FOR PULSED HIGH CURRENT

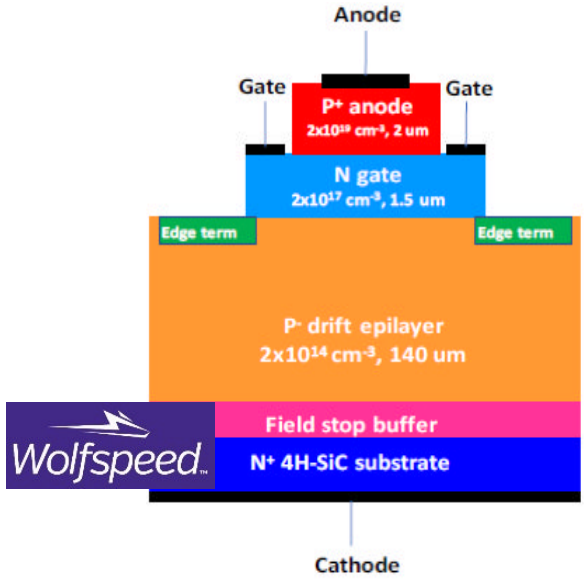
- Embedded termination for simpler processing and greater blocking yield
- 140-µm blocking layer for 15 kV
- Ni ohmic annealed at elevated temperature for stable V_f at high-current densities
- 1450 C lifetime enhancement to reduce V_f and improve latch-up and holding current
- Optimized epi surface treatment process to maintain high-voltage blocking



N-drift 1.0 cm², 15-kV SiC PiN diode



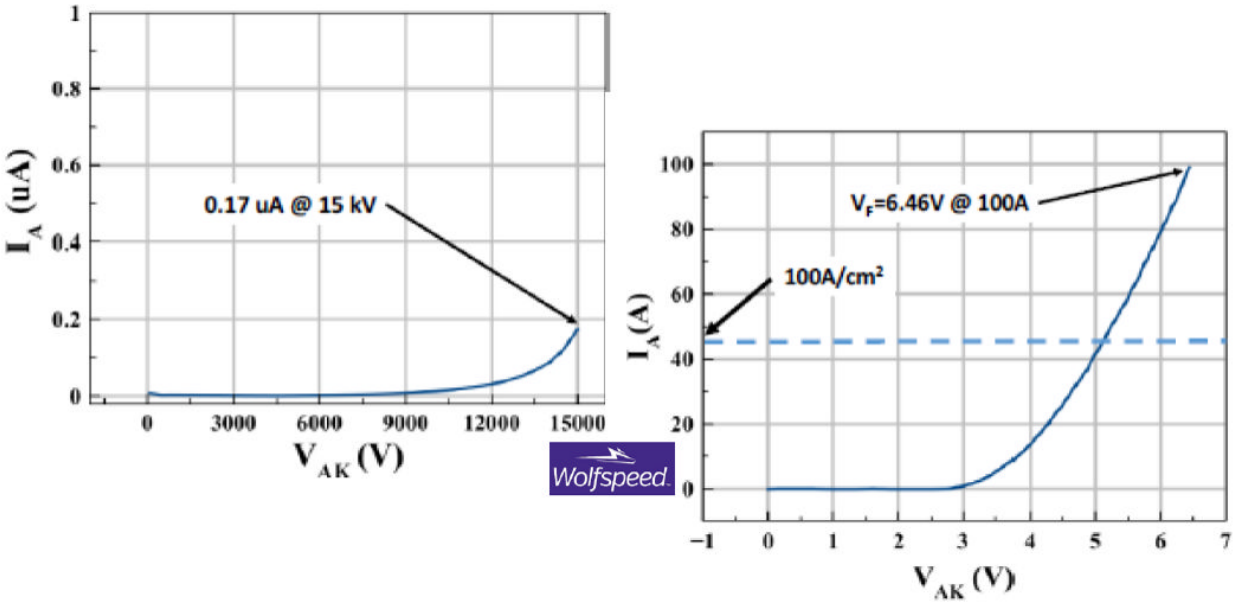
N-doped 1.0 cm², 15-kV SiC thyristor

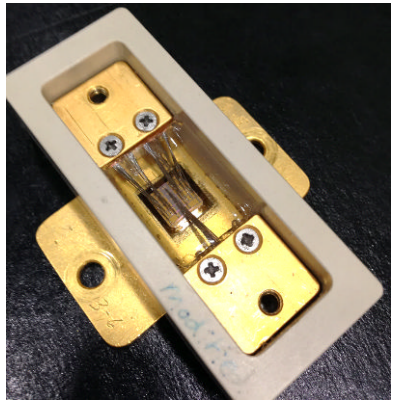


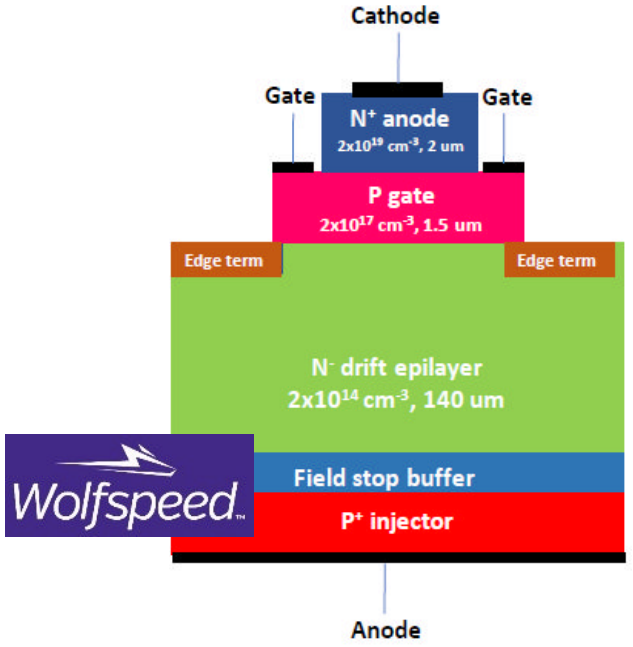
P-doped 1.0 cm², 15-kV SiC thyristor

N-DOPED EPI DESIGN AND EXPECTATIONS

- The 15 kV SiC n-thyristor utilizes an identical device structure to that used for the p-thyristor, except the polarity of the epilayer is reversed and the p+ injector layer at the anode was thinned.
- Fabrication process includes lifetime enhancement oxidation at 1450 C and epi surface treatment prior to gate and cathode epi growth.
- It was projected that carrier lifetimes of 15–20 µs in the n-epi would lead to lower V_f and greater lateral current spreading velocity.



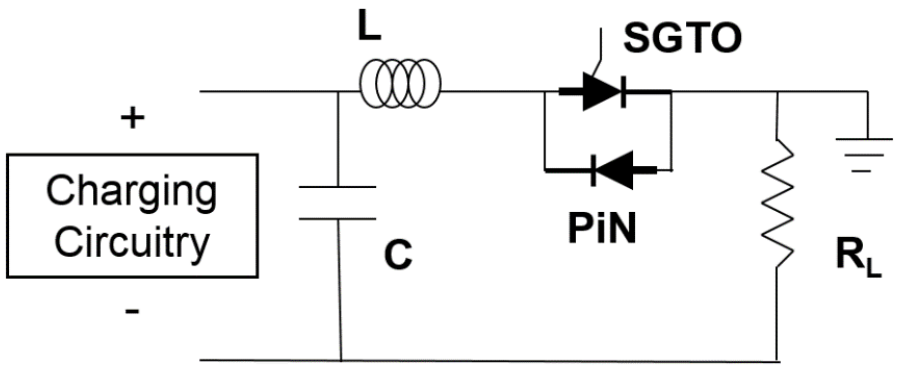




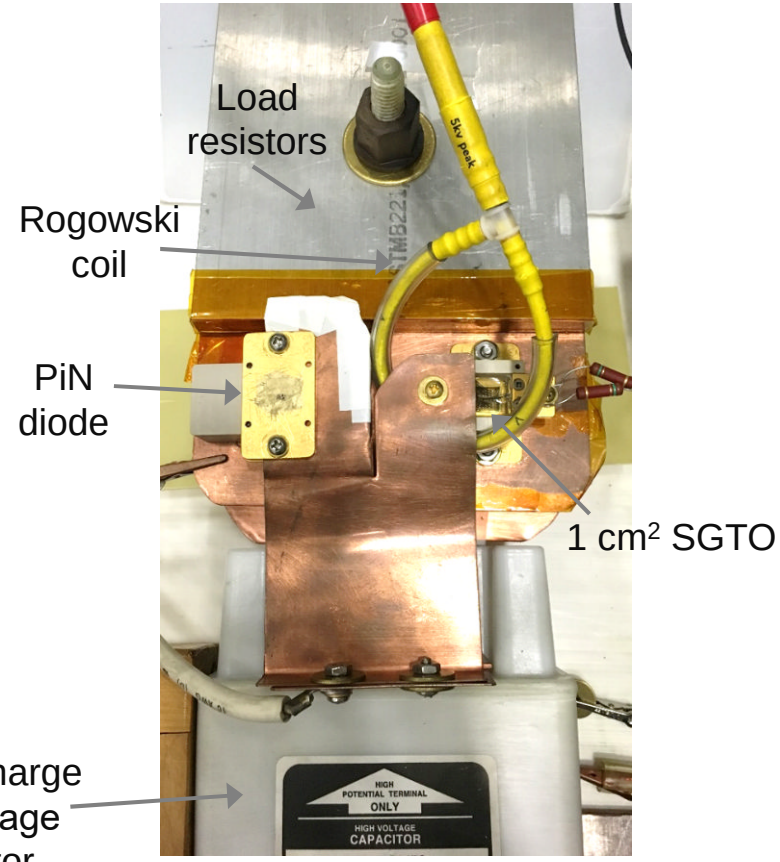
N-doped 1.0 cm², 15 kV SiC thyristor

METHODOLOGY

- Design circuit for high *dI/dt* (emphasis on *t*)
- Investigate gating techniques
- Investigate minimum switching period (charge, switching, recovery)
- Modify circuitry for higher V, burst rate
- Optimize gating controls and data acquisition
- Identify limits and align with applications



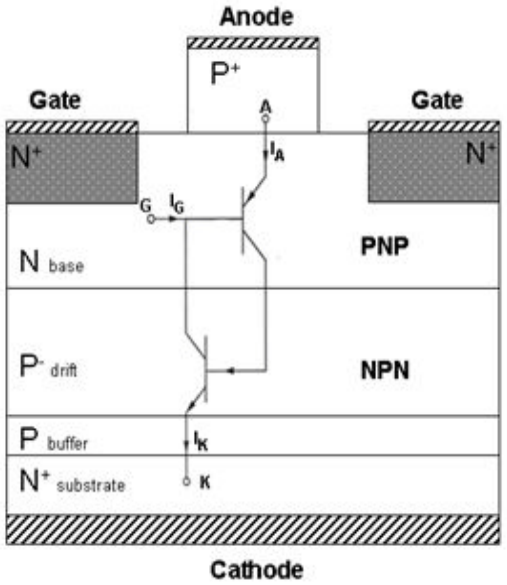
General schematic of the capacitor discharge circuit. The PiN diode was later removed to allow thyristor to self-commutate.



TURN-ON DELAY AND *DI/DT*

Contributing Factors:

– base width of each transistor
– diffusion rates
– current density
– charge
– device geometry



General cross section of a thyristor and equivalent transistor circuit

Turn-on Delay Time

$$t_d = \frac{1}{2}\frac{{W_p}^2}{D_n} + \frac{1}{2}\frac{{W_N}^2}{D_p}$$

Spreading Velocity

$$v_s \propto \frac{J}{q}\left(\frac{1}{W_N + W_p}\right)\sqrt{\frac{\tau_{HL}}{D_a}}$$

W_P: p-type base width
W_N: n-type base width
D_n: electron diffusion rate
D_p: hole diffusion rate
J: cathode current density
q: charge
T_{HL}: carrier lifetime
D_a: ambipolar diffusion coefficient

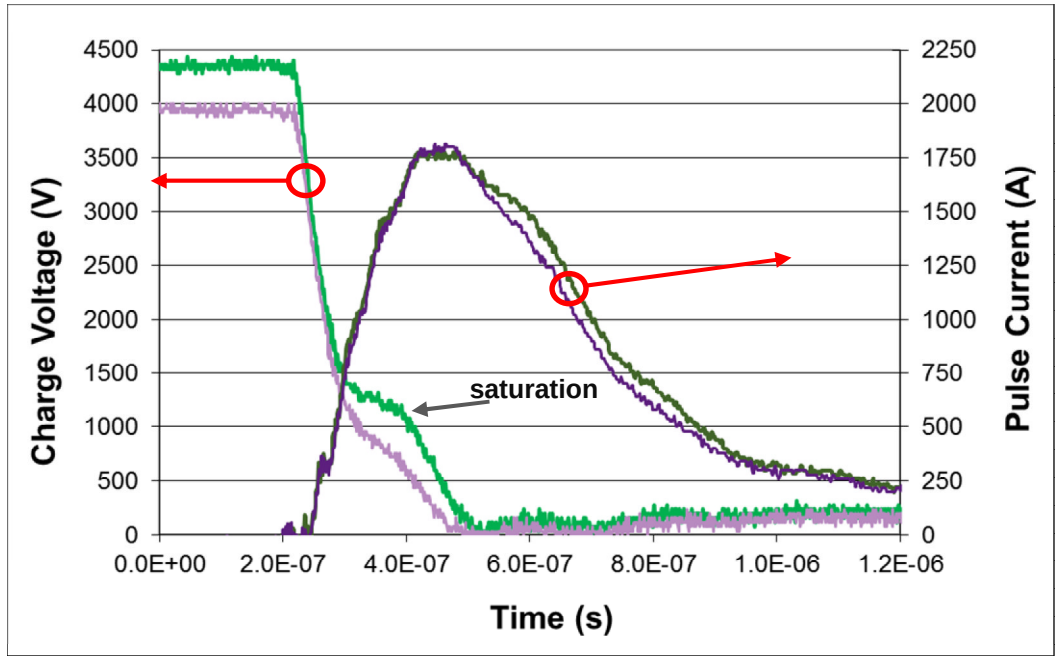
Eq. Reference: B.J. Baliga, *Fundamentals of Power Semiconductor Devices*, PWS Publishing, Boston, 1996.

TURN-ON DELAY AND *DI/DT*

Importance of Understanding Performance Limitations at Initial Turn-on:

- Factors into controls and trigger timing in fast-response applications
- Defines the maximum operating frequency or pulse rate
- Enables comparison of different device designs under extreme conditions (moderate speed combined with high power)

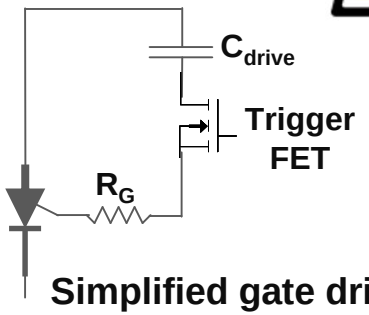
Example of saturation limitation at initial turn-on for 10-kV thyristor, manifested as elevated on-state voltage (power dissipation) and negligible increase in peak current:



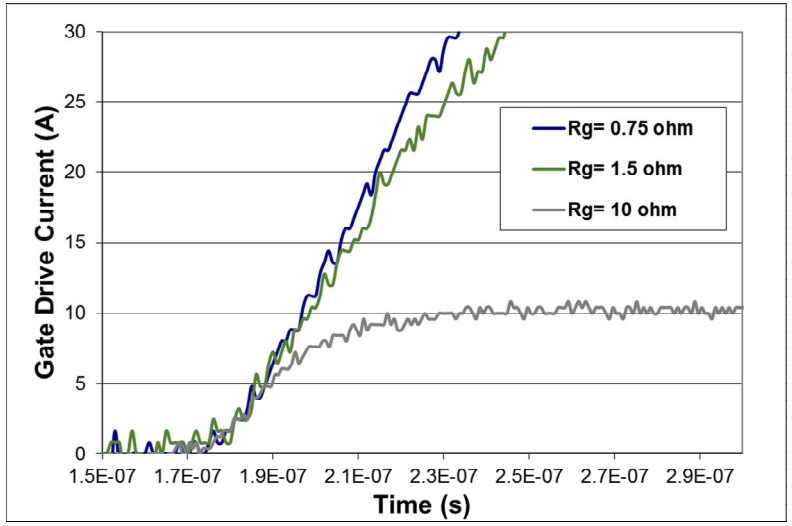
MINIMUM TURN-ON DELAY

Relevance

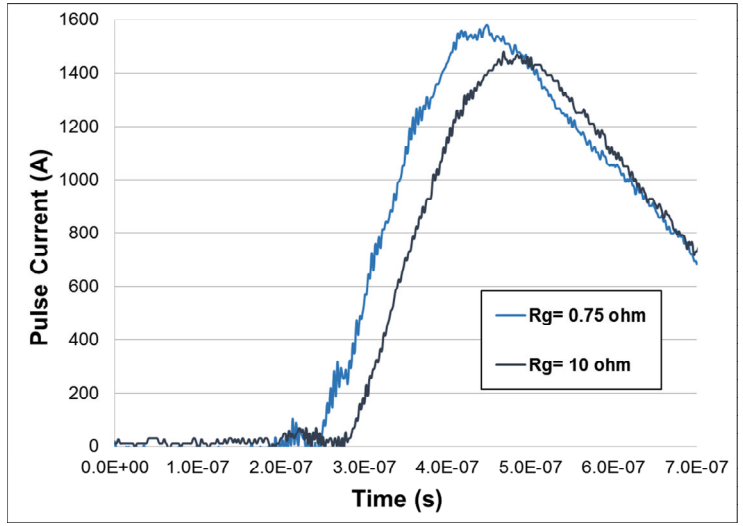
- Compares delays for different voltage-blocking ratings/epi designs
- Factors into controls and trigger-timing in fast-response applications
- Sets a limit on the operating frequency



Simplified gate drive configuration

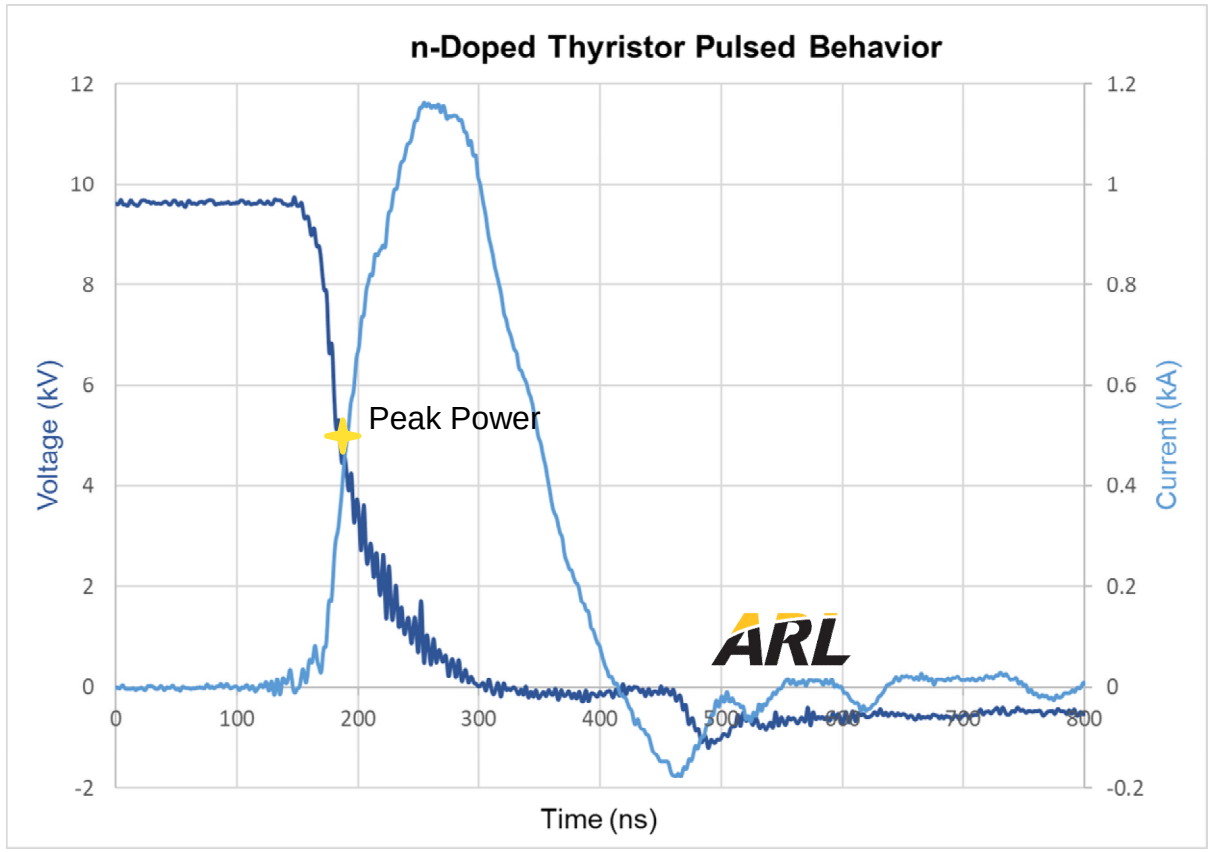


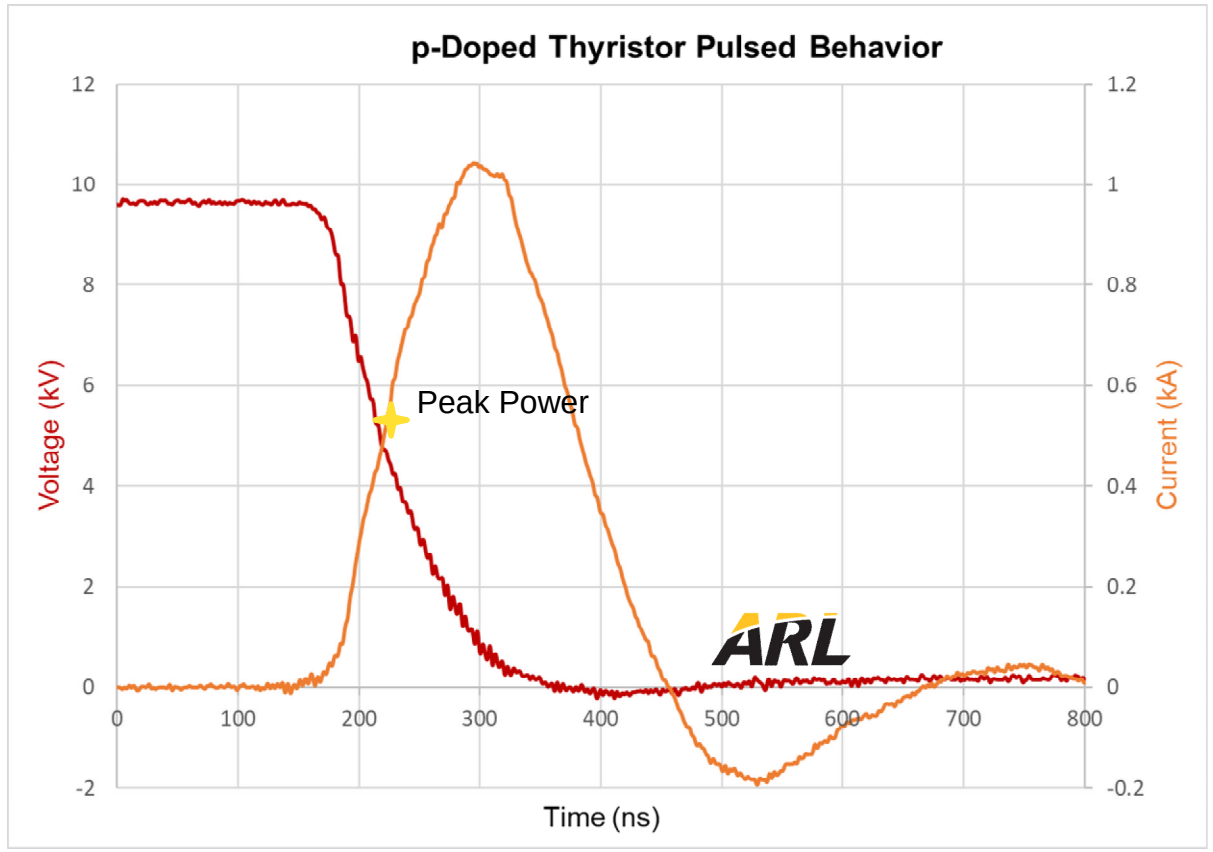
Rising edge of applied gate current: 200 A/µs for Rg=10 ohm, 400 A/µs for lower gate resistor values.



Increasing rising edge to 400 A/µs enabled SGTOs to turn on 25 ns earlier, starting to conduct pulse current at 75 ns delay after initial applied gate current.

N-TYPE, P-TYPE DIRECT COMPARISON





Full width at half maximum (FWHM): 145 ns
Peak current: 1.1 kA
t_d gate-to-peak: 110 ns

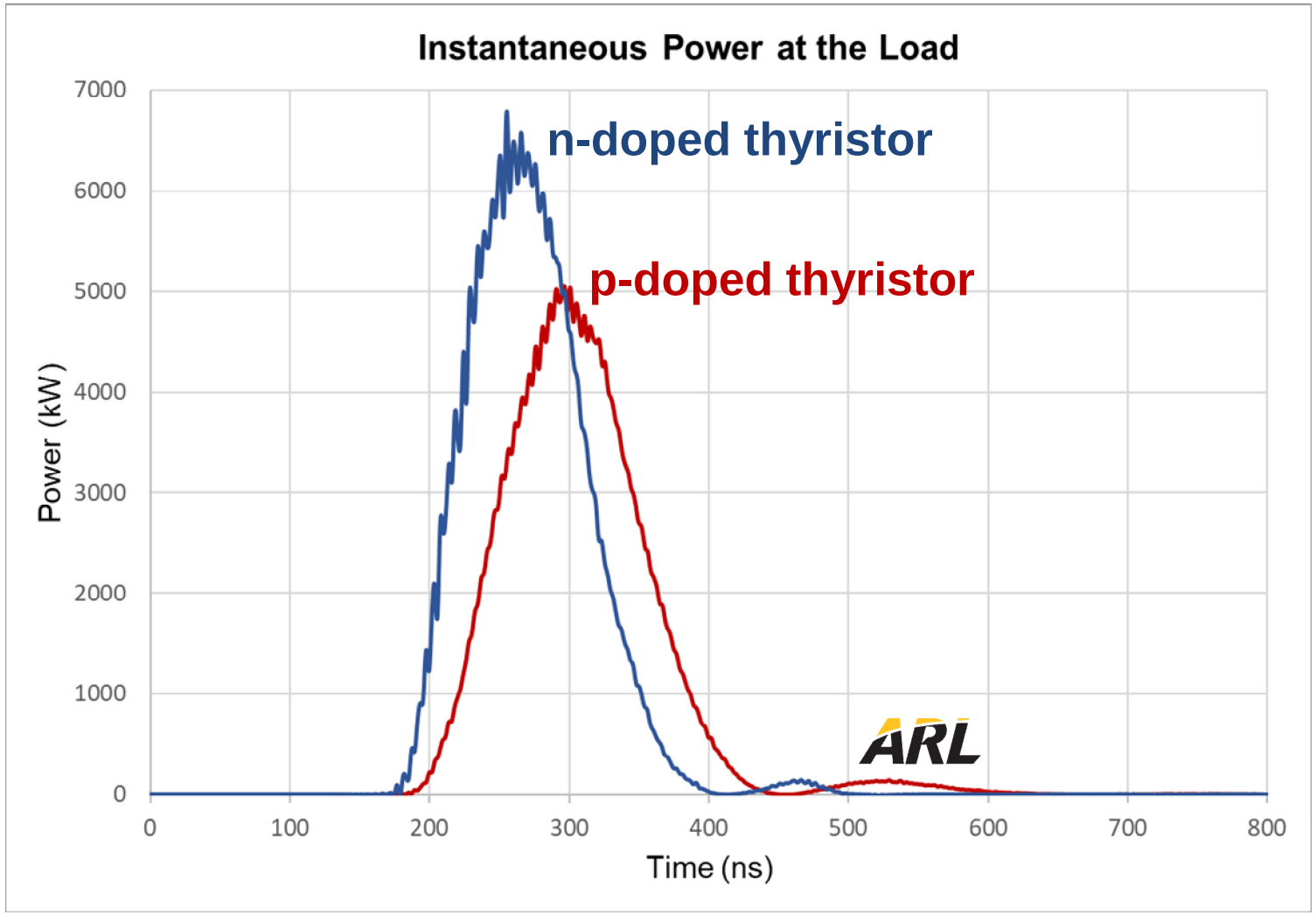
dI/dt (10-90%): 15.4 kA/µs
Peak power: 2.2 MW

FWHM: 160 ns
Peak current: 1.0 kA
t_d gate-to-peak: 160 ns

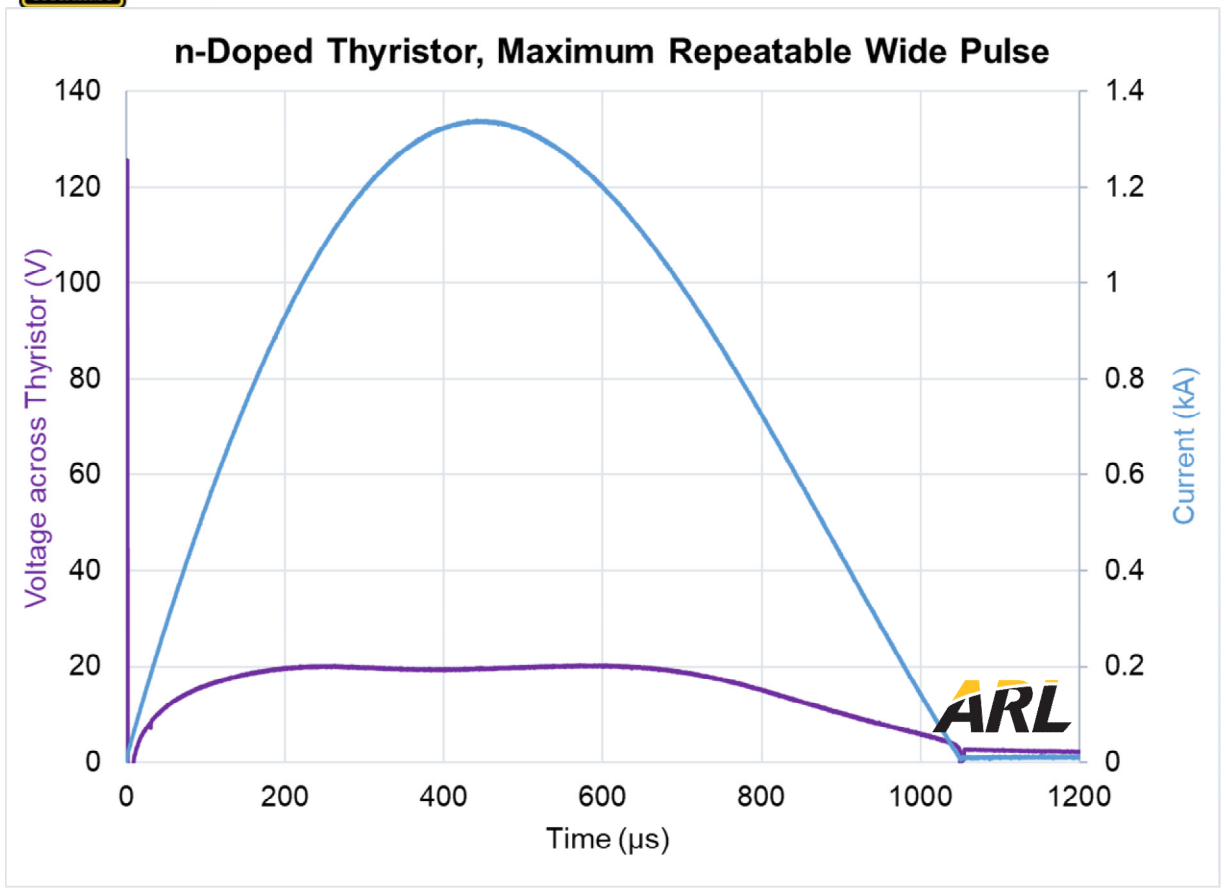
dI/dt (10-90%): 10.3 kA/µs
Peak power: 2.6 MW

N-TYPE, P-TYPE DIRECT COMPARISON

The greater lateral current-spreading of the n-doped thyristor resulted in lower switching loss at narrow pulse, transmitting 30% more power to the load.

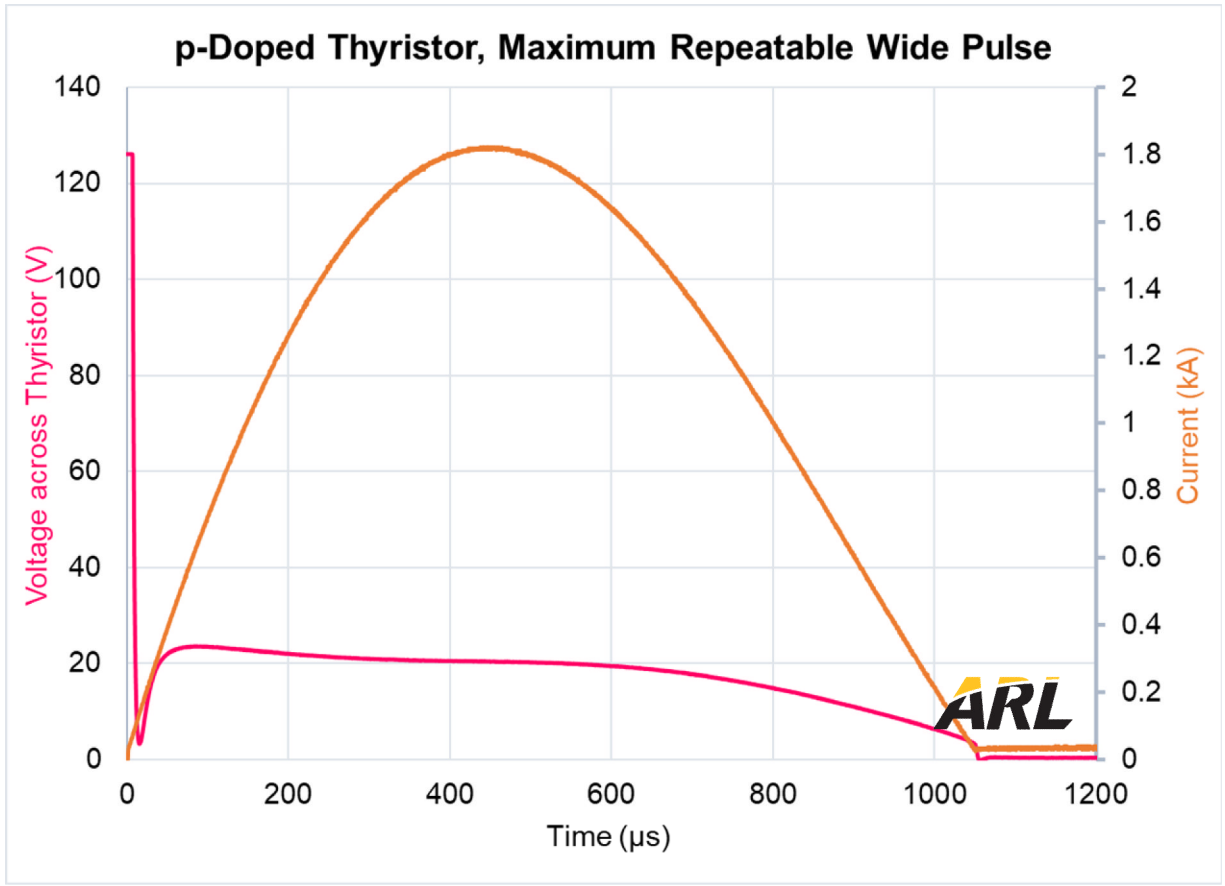


N-TYPE, P-TYPE DIRECT COMPARISON



FWHM: 680 µs
Peak current: 1.3 kA
On-resistance: 14 mΩ

I^2t: 0.92 x10^3 A^2s
Peak power: 25 kW



FWHM: 680 µs
Peak current: 1.8 kA
On-resistance: 11 mΩ

I^2t: 1.7 x10^3 A^2s
Peak power: 36 kW

KEY TAKEAWAYS

- For rapid, low-energy (<1 J) discharge, the n-doped thyristor had lower switching loss, peaking 50 ns earlier than the p-doped thyristor, transmitting 30% more instantaneous power to the load.

- At higher-energy (400 J), higher-action switching, the p-doped thyristor had lower conduction loss, enabling almost 40% higher current density.

- Both designs could use further optimization to increase lateral current spread at turn-on and reduce overall on-resistance.

PATH FORWARD

- Refine n-thyristor doping and layout
- Improve high-current package contact for high *dI/dt*
- Explore further application space for the high-voltage thyristor

RELEVANT PUBLICATIONS

A. Ogunniyi, H. O'Brien, S. Ryu, and J. Richmond. "High-power pulsed evaluation of high-voltage SiC n-gto," 2019 IEEE 7th Workshop on Wide Bandgap Power Devices and Applications, pp. 425-429, 2019.

B. H. Ryu, et al. "15 kV n-GTOs in 4H-SiC," Materials Science Forum, 963, pp. 651-654, 2019.

H. O'Brien, A. Ogunniyi, and M. Hinojosa. "Overview of SiC high-voltage switch development and evaluation at the U. S. Army Research Lab," Proc. 2017 Directed Energy Symposium, 2017.

H. O'Brien, A. Ogunniyi, W. Shaheen, and S.-H. Ryu. "Turn-on of high-voltage SiC thyristors for fast-switching applications," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 4, no. 3, pp. 772-779, Sept. 2016.